ABSTRACT OF THE DISCLOSURE

A solid-state image sensing apparatus which can improve the S/N ratio without enlarging the chip area in both of the mode in which pixel signals are summed and the mode in which pixel signals are not summed is provided. The solid-state image sensing apparatus includes an image sensing region 510 in which a plurality of unit cells 500 is laid out two-dimensionally, the first vertical signal line 520, a row selection circuit 530, a column selection circuit 560, a horizontal signal line 570 and a signal processing unit 100, having a sampling capacitors which accumulate signals corresponding to amplified signals of the unit cells, which selects the case of summing the signals or the case of not summing the signals, wherein the capacitance of the sampling capacitor which accumulates a signal corresponding to an amplified signal of a unit cell for each row when the sum is performed is smaller than the capacitance required for reading out the signal from said capacitor.